



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,841	11/13/2003	Rajesh Sundaram	ITL.1062US (P17921)	2553
21906	7590	03/06/2006	EXAMINER	
TROP PRUNER & HU, PC 8554 KATY FREEWAY SUITE 100 HOUSTON, TX 77024			LE, THONG QUOC	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

87

Office Action Summary	Application No.	Applicant(s)	
	10/713,841	SUNDARAM ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-5,7,9-11,14-19,22-25 and 27-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 22-25 and 27-30 is/are allowed.
- 6) ☒ Claim(s) 1,3-5,7,9-11,14-19 and 31-33 is/are rejected.
- 7) ☒ Claim(s) 34-37 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Amendment filed on 12/20/2005 has been entered.
2. Claims 1, 3-5,7,9-11,14-19,22-25,27-37 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1,3-5,7,9-11,14-19,31-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Bedarida et al. (U.S. Patent No. 6,804,148).

Regarding claim 10, Bedarida et al. disclose an apparatus comprising':

a decoder (ABSTRACT) to supply a negative voltage to a deselected address line of a memory array (ABSTRACT), the decoder comprising a first transistor (Figure 2, 204, [0031]) of a first polarity coupled to receive a negative control voltage ([0031]) and the negative voltage and to pass the negative voltage to the deselected address line

and a second transistor (Figure 2, 206, [0031]) of a second polarity coupled to the first transistor and the deselected address line to pass a program pulse to the deselected address line if it becomes a selected address line ([0032-0033],[0037]).

Regarding claim 11, 14-16, Bedarida et al. disclose wherein the decoder is further coupled to supply a positive voltage to the same address if it is selected to be programmed (Figure 3A, WS=POS), and a pre-driver circuit to disable the first transistor if the deselected address line becomes a selected address line ([0034], [0038]), and a plurality of memory cells coupled to the decoder via the deselected address (Figure 1A), wherein the plurality of memory cells comprise a multi-level cells of a flash memory (ABSTRACT).

Regarding claim 17, Bedarida et al. disclose an article comprising a machine-readable storage medium containing instructions that if executed enable a system to:

supply a negative voltage to at least one deselected wordline of a memory array ([0031]); and provide a negative control voltage to a substrate of a transistor coupled to pass the negative voltage to the at least one deselected wordline (Figure 4B-4D, NEG).

Regarding claims 18-19, Bedarida et al. comprising instructions that if executed enable the system to supply a positive voltage to a selected wordline of the memory array to program the selected wordline while the negative voltage is supplied to at least one deselected wordline ([0032-0036]), and comprising instructions that if executed enable the system to supply the negative voltage to all wordlines of the memory array except the selected wordline ([0042]).

Regarding claim 31, Bedarida et al. disclose wherein the first transistor comprises a well coupled to receive the negative control voltage, a source terminal coupled to receive the negative voltage, a drain terminal coupled to pass the negative voltage to the deselected address line (Figure 5B-D, 504B, well, source, drain coupled negative voltage in unselected).

Regarding claims 32-33, Bedarida et al. disclose a negative switch coupled to provide the negative voltage and a negative control voltage to the decoder, and a second decoder coupled to another wordline of the memory array ([0021, Figures 6A-B).

Regarding claims 1, 3-5,7,9, the apparatus discussed above would performed the method in claims 1, 3-5,7,9.

Allowable Subject Matter

5. Claims 22-25,27-30 are allowed.

Claims 22-25, 27-30 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Bedarida et al. (Pub. U.S. Patent No. 2004/0076037), and others, does not teach the claimed invention having a wireless interface coupled to the nonvolatile memory array.


6. Claims 34-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 34-37 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Bedarida et al. (Pub. U.S. Patent No. 2004/0076037), and others, does not teach the claimed invention having a pre-driver circuit to control an intermediate node coupled to a gate terminal of the first transistor and a gate terminal of the second transistor as claim 34-36 disclosed, and a first pre-driver circuit coupled to the at least one deselected wordline to pass a positive control voltage to a first control node coupled to a first pair of transistors of different polarities, and to control a second pre-driver circuit coupled to the selected wordline to discharge a second control node coupled to a second pair of transistors of different polarities as claim 37 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Thong Q. Le
Primary Examiner
Art Unit 2827

2/27/2006